Request for Proposal

Procurement of Services for Upskilling Training Program (USTP) for the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I"

Central Region (Punjab)

A (01)/PSEB/2026-10

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Contents

1. Introduction to PSEB

Pakistan Software Export Board (PSEB) is an entity under the Ministry of IT & Telecom mandated to act as One Stop Shop on behalf of Government of Pakistan and ensuring of sustainable growth, development of the industry and enhancing of IT & ITeS exports. One of the objectives of PSEB is availability of skilled resource equipped with latest technologies for the IT Industry. In order to help increase the employability and to fill the supply gap for industry-ready skilled resource, PSEB under the guidance of Ministry of IT and consultation with IT Industry is initiating a series of HR development program, one of the said programs is equipping of the IT professionals and ICT & Non-ICT graduates with latest technologies by the ICT Industry Professionals which will help in enhancing the number and quality of HR workforce available to Pakistan IT & ITeS industry

2. Introduction to the Project

The National Semiconductor Human Resource Development Program (NSHRDP) is a strategic initiative aimed at building a skilled and globally competitive workforce in semiconductor design and development. The program seeks to bridge the talent gap in Pakistan's IC design ecosystem by launching structured academic and upskilling programs across universities and training institutes. Through targeted education, hands-on training, and industry collaboration, the project aims to enable local talent to contribute to global chip design, foster innovation, and attract investment in Pakistan's emerging semiconductor sector.

This procurement directly supports overall objective of the project, including:

- **Component I: Semiconductor Education & Research Clusters (SERCs)**: Focused on formal academic training, this component aims to strengthen undergraduate (BS/BE) and postgraduate (MS/PhD) programs in electronics, electrical engineering, and computer engineering disciplines, through access to state-of-the-art Electronic Design Automation (EDA) tools and compute infrastructure.
- **Component II: Upskilling Training Programs (USTPs):** Targeting professionals and industry practitioners, this component seeks to deliver fast-track, modular training in digital and analog chip design, verification, layout, and embedded systems, aligned with real-world industrial demands.

- **Component III: Centralized Electronic Design Automation (EDA) Tools:** This component plays a critical enabling role by providing shared access to industry-standard EDA software, silicon IP repositories, and remote design environments through a centralized cloud-based infrastructure. This component ensures that both SERCs and USTPs have the necessary digital tools and support to deliver high-quality semiconductor education and training.

3. Objectives of Procurement

The primary objective of this procurement is to engage capable and experienced academic institutions, training providers, and technical organizations in the design, development, and delivery of outcome-driven, structured training programs focused on semiconductor IC chip design and

verification. These programs aim to address the growing demand for skilled semiconductor professionals in Pakistan and align the local talent pool with international industry standards.

Specifically, this procurement of trainings services seeks to:

3.1. Build a Scalable Semiconductor Talent Pipeline

Launch and institutionalize tiered training programs (Foundation, Specialized, Expert) that progressively upskill engineering graduates—from basic semiconductor knowledge to project-ready and expert-level capabilities. This includes integrating industry standard EDA tools, industry-standard methodologies, and real-world design practices into the training curriculum.

3.2. Bridge the Skills Gap in IC Design and Verification

Address the critical shortage of hands-on experience among engineering graduates, which has previously led companies to invest heavily in costly and time-consuming in-house training. By standardizing and externalizing this process through national training initiatives, the burden on industry is reduced and new talent can be integrated more efficiently.

3.3. Enhance Industry Readiness and Employability

Develop a workforce that is deployable from day one through hands-on exposure to industry tools and workflows, collaborative design projects, and domain-specific specialization tracks. Procurement will support training models that include direct industry engagement, mentorship, and job placement.

3.4. Promote Inclusive and Decentralized Access to Semiconductor Training

Encourage participation from institutions across geographic regions to democratize access to specialized training. This will enable a more diverse and inclusive talent pipeline and support national efforts to build semiconductor clusters beyond traditional urban centers.

3.5. Accelerate Ecosystem Development for Fabless IC Design

By seeding trained professionals at multiple levels of expertise (foundation, specialist, expert), this initiative aims to create an enabling environment for startups, multinational R&D centers, and local design houses to scale operations, form seed teams, and undertake complex design projects locally.

3.6. Enable Outcome-Based Funding Linked to Measurable KPIs

Training providers will be held accountable through clearly defined performance metrics, including placement rates, project completion, and industry endorsement. This procurement process will enforce standards and track outputs, ensuring that public investment yields measurable economic and technological outcomes.

3.7. Catalyze Public-Private-Academic Collaboration

Leverage partnerships between academia, government, and the private sector to align curricula, optimize resources (e.g., shared EDA labs), and strengthen Pakistan's positioning in the global semiconductor value chain.

Through this RFP, NSHRDP seeks committed firms/consortiums with proven experience, and the capacity to deliver USTP program solutions with comprehensive trainings.

4. Scope of Work

4.1 Level-I (Foundation Course): IC Chip Design and Verification

The selected training institutions/ partners will be responsible for the design, delivery, monitoring, and evaluation of structured upskilling programs of Level-I (Foundation Course) trainings with enhanced course curriculum on IC Chip Design and Verification training. This program will be executed under Component II of the National Semiconductor Human Resource Development Program (NSHRDP), and aim to bridge the skills gap in Pakistan's semiconductor ecosystem by preparing engineers for industry-aligned, job-ready roles in chip design and verification.

The programs will be designed to include industry-relevant curricula, hands-on labs, project-based learning, and certification linked to performance. The institutions are expected to ensure high-quality instruction, learning outcomes on international standards, and strong linkages with industry for employment, mentorship, and feedback integration.

4.2 Training Delivery Model

The trainings will be conducting simultaneously in the region, as follows:

a. Central Region (Punjab)

Note: The participating firms should comply with above requirement, by identifying, training locations / centers within geographical boundaries as mentioned above.

4.3 Trainings distribution

(Central-Region)
200 Trainees

a. The number of trainees mentioned against the region may be changed based on the availability of funds and trainees' enrollment.
b. These numbers shall be treated as program target to guide allocation across the region. Bidders are expected to propose trainee intakes that are realistic, evidence-based, and aligned with their institutional capacity, infrastructure readiness, and industry linkage plans.
c. Flexibility within reasonable limits is allowed to ensure quality delivery and avoid inflated or fictitious claims. Minor variations in cohort sizes in the Central Region (Punjab) may be proposed, provided that:

i. The per-trainee cost model remains consistent.
ii. The proposed numbers stay close to the above targets and maintain regional balance.
iii. Employability outcomes remain the central measure of success.

Final approval of cohort allocations will rest with the **Project Steering Committee** to ensure fairness, quality, and alignment with national program objectives.

4.4 Student eligibility criteria:

Graduates 2023 onwards, of following disciplines will be eligible to participate in the trainings:

Electronic Engineering, BS/M.Phil Electronics, Software Engineering, Computer Engineering, Electrical Engineering or the related disciplines as approved by the competent authority.

4.5 Eligibility Condition to Participate in Bidding Process:

No single firm or entity shall be eligible to participate independently. Participation will only be permitted through a consortium comprising academia, companies engaged in chip/semiconductor-related business, and established training centers with demonstrated experience in delivering high-tech training programs. Lead partner or one of the consortium partners must have presence in the Central Region (Punjab).

4.6 Level-1: Foundation Training (enhanced course outlines)

Objective:

- To prepare fresh engineering graduates with essential theoretical and practical knowledge that is typically missing from undergraduate curricula, in addition to hands on training fundamentals of chip design and verification methodologies/techniques, making them job-ready for entry into the semiconductor domain. Below is the outline of intended trainings spanned over 04 months and covered in max 500 hours to be followed by the selected consortium(s). The consortium is to submit a comprehensive/detailed course details to be delivered. The respective authority will review the detailed curriculum in line with the below outlines and course objectives and approve or amend, as deemed appropriate.
- Digital Design & Verification Boot Camp-Level 1 - (4 Months Duration)
- Target: Electronic Engineering, BS/M.Phil Electronics, Software Engineering, Computer Engineering, Electrical Engineering or the related disciplines, as approved the competent authority, aiming for entry level position in the semiconductor industry.
- Aligned with the curriculum outlined in the RFP, the consortiums may propose enhanced curriculums but the curriculum to roll-out is subject the approval of Project Steering Committee.
- Curriculum Alignment – Split after 6 weeks into two tracks:
    a. Digital Design Verification
    b. RTL & Backend Design

Month 1 – Foundations

Goal: Build core programming and digital design skills.

C/C++ for Hardware Engineers

- Basics: syntax, control structures, pointers, arrays, strings
- Data structures: linked lists, queues, stacks, hash tables
- OOP concepts: inheritance, polymorphism, virtual functions, lambdas
- Low-level coding: bitwise operations, memory-mapped I/O simulation
- Lab: Cache simulator in C++

Digital Logic Design Fundamentals

- Boolean algebra, combinational & sequential logic
- Finite State Machines (Use relevant tools, to deliver the module)
- Timing concepts: setup/hold, metastability, clock domain crossing
- Basic protocols: UART, SPI, I²C
- Lab: FSM-based UART controller (behavioral simulation)

Month 2 – RTL Design & Industry Protocols

Goal: Master synthesizable Verilog RTL coding and learn common interface protocols.

RTL Design with Verilog *(Dedicated Module)*

- Modules, ports, parameters, generate blocks
- Combinational logic (always @(*), blocking assignments)
- Sequential logic (always @(posedge clk), non-blocking assignments, resets)
- FSM design patterns, avoiding latches
- Hierarchical design & parameterization
- Tool Flow:
    - Simulate RTL in tools (Use relevant tools, to deliver the module)
    - Lint (Use relevant tools, to deliver the module)
    - Synthesize (Use relevant tools, to deliver the module)
- Lab: ALU, FIFO, and a 2-way set associative cache controller

Industry Protocols & Integration

- AMBA bus standards: AXI, AHB, APB
- Protocol design considerations
- Simple DMA engine design
- Lab: AXI-lite slave RTL module with APB bridge

Month 3 – ASIC Flow, SystemVerilog & Verification

Goal: Transition to verification coding and understand ASIC tool flows.

ASIC Design Flow (Use relevant tools, to deliver the module)

- RTL → GDSII overview
- Linting & CDC analysis
- Synthesis & constraints
- Static Timing Analysis
- Floorplanning & routing basics
- Lab: Synthesize AXI-APB bridge, run STA, basic floorplan,

for Design & Verification (Use relevant tools, to deliver the module)

- Synthesizable vs non-synthesizable constructs
- Interfaces, modports, virtual interfaces
- OOP in SV, constrained randomization
- Coverage: functional & code

- Assertions (SVA) basics
- Lab: Layered testbench for FIFO in SystemVerilog (Use relevant tools, to deliver the module)

Month 4 – Verification & Final Project

Goal: Build a UVM verification environment and complete a full design + verification cycle.

UVM (Universal Verification Methodology)

- Testbench architecture, agent, sequencer, driver, monitor
- Factory & configuration methods
- Sequence items & stimulus generation
- Scoreboarding & coverage closure
- Register Abstraction Layer (RAL)
- Lab: UVM environment for AXI-APB bridge or FIFO

Final Integrated Project *(Student Choice)*

Options:

- Protocol controller (AXI-Stream to FIFO)
- DSP accelerator (e.g., FIR filter)
- Memory controller (SRAM/DDR interface, simplified)

Optional: Extend a small RISC-V core with a custom instruction Flow:

- Frontend: RTL coding, linting, synthesis
- Backend: STA (PrimeTime), simple floorplan
- Verification: UVM environment, functional & code coverage, assertions (Use relevant tools, to deliver the module)
- **Deliverables:**
    - RTL & verification code in Git repo
    - Synthesis scripts & reports
    - Coverage reports
    - Final documentation & presentation

Optional Short Module – Processor Architecture

(For students interested in CPU design; 1–1.5 weeks)

- Basic 3/5-stage pipeline
- Instruction decode, execute, memory, writeback
- Hazards & forwarding
- Integration with AMBA bus
- Lab: Add a simple custom instruction to a small CPU core

Additional Skills

- Coverage closure strategies
- Writing design & verification specifications
- Code review best practices

4.7 General Responsibilities for All Training Providers' Consortium

Following responsibilities will apply:

- **Selection Process:** Conduct open, merit-based admissions (with geographic inclusivity)

- **Quality Assurance:** Follow national standards and international benchmarks for content and delivery.
- **Monitoring & Reporting:** Submit weekly reports, maintain attendance logs, record feedback.
- **Facilities:** Ensure access to well-furnished labs equipped with high specific workstations, EDA tools, internet, and technical support.
- **Assessment:** Develop pre- and post-assessments, quizzes, capstone evaluations
- **Placement & Impact Tracking:** Report employment stats post-training, maintain alumni database
- **Coordination with PIU:** Attend review meetings, respond to compliance checks, facilitate audits.

5. Proposal Requirements

All bidding firms/consortiums are required to submit a complete proposal package comprising a Technical Proposal and a Financial Proposal separately on EPADS). Any proposal that is incomplete, or fails to comply with the prescribed format and submission requirements, shall be rejected without further evaluation.

5.1 Technical Proposal

The Technical Proposal must demonstrate the applicant's understanding of the program, their technical capacity to deliver the training, and a clear roadmap for execution and outcomes. It should include the following sections:

5.1.1 Institutional Profile

- Overview of the applying organizations/consortium
- Legal status and relevant registrations (HEC, SECP, etc.)
- Vision, mission, training expertise and relevance to semiconductor industry
- Key personnel and their qualifications

5.1.2 Relevant Experience

- Summary of past experience in delivering - IC design training programs.

5.1.3 Proposed Training Plan

- Training levels being applied for Level-1, with enhanced course curriculum spanned over 04 months and covered in max 500 hours.
- Proposed curriculum and module outlines.
- Weekly training schedule and structure (lab vs lecture hours)
- Training methodology (hands-on, blended, flipped, etc.)
- Certification plan (pre/post assessments, project review, exams).

5.1.4 Trainer and Staff Details

- Detailed CVs with qualifications and semiconductor-specific experience.
- Availability and commitment duration.

5.1.5 Lab Infrastructure and Tool Access

- Description of on-site or virtual lab facilities.
- Availability or access plan for EDA tools.
- Number of workstations, licenses, and usage plan.

5.1.6 Partnerships and Industry Linkages

- Letters of support or signed MoUs with companies for project collaboration and trainees' placement.
- Strategy for involving industry experts in mentorship or curriculum input.
- Placement support model.

5.1.7 Monitoring and Reporting Mechanism

- Tools or systems for trainee tracking, attendance monitoring, and feedback collection.
- Format of progress and performance reports.
- Mechanism for evaluating program impact.

5.1.8 Sustainability and Scale Plan

- Plan for sustaining and scaling the training beyond the current cycle.
- Institutional commitment to integrate into regular offerings (if applicable).

5.2 Financial Proposal

The Financial Proposal must present a transparent, detailed, and justifiable budget for the proposed training programs on per trainee basis. It should include:

5.2.1 Budget Breakdown

- The per trainee cost shall include the cost of each element involved in the delivering the specified trainings like, Trainer and staff honorarium, Lab infrastructure and operational costs, Software/tools access or licensing, Utilities and overheads, Materials and printing, Monitoring and administration. Trainee stipend is not to be included in the per trainee cost.

5.2.2 Batch-wise Cost Summary

- Cost estimates based on proposed batch size (maximum trainees per batch shall not exceed than 40).
- Multiple batch scenarios (if applicable).

5.2.3 Payment Milestones

Sr. #	Deliverables	% age of Contract Amount
1	Submission of all three: 1. Training Curriculum 2. Outreach + Engagement to conduct test for selection of most suitable trainees 3. Final announcement of selected trainees	**15%**
2	Completion of 33% trainings hours	**20%**
3	Completion of 66% of training hours	**20%**
4	Completion of 100% training hours	**20%**
5	Post Training Assistance and 60% Job Placement • 15% Payment on 40% job placement (within 90 days of training completion) • 10% Payment on 20% of remaining job placement	**25%**

Only those proposals that meet the eligibility criteria outlined in Section 5.8 and are deemed technically responsive (achieving the minimum qualifying score of 70% in the technical evaluation) will proceed to the financial evaluation stage.

5.3 Financial Evaluation (Total Weight: 20%)

Financial proposals will be evaluated for cost-efficiency and value-for-money.

Note: The lowest responsive bid will receive full marks; others will be scored proportionally using a formula (e.g., [Lowest Bid ÷ Bidder's Cost] × 20).

5.4 Final Selection

The final score will be calculated as follows:

- **Technical Proposal:** 80%
- **Financial Proposal:** 20%
- **Total Maximum Score:** 100 Points

5.5 Consortium Participation:

Participation in the subject RFP will be through a consortium comprised entities complying eligibility criteria. Consortiums may include academic institutions, training providers, and industry partners, combining their expertise to deliver various aspects of the training program. A formal consortium agreement outlining roles, responsibilities, must be submitted with the proposal. The

lead local partner will be solely accountable to the PIU for coordination, reporting, and financial compliance.

5.6 Mandatory Eligibility Criteria Checklist

Before the Bidders submit their Proposals, within the stipulated time mentioned in this Request for Proposal document, Bidders are required to make sure that following mandatory requirements of this RFP document are fulfilled. These requirements must be furnished at the time of submission of Proposal. Non-submission of any one of the following applicable requirements shall result in disqualification:

Sr#	**Mandatory Eligibility Criteria Checklist** (If compliant, please check, otherwise put a Cross in the Mark Column)	**Mark (Yes/No)**
1.	Proof of Certificate of Incorporation or Registration or equivalent (applicable on lead and all JV Partners).	
2.	Proof of NTN Registration (applicable on lead and all JV Partners, in case of exemption of any partner, the relevant exemption from relevant authority should be attached in proposal with proper justification).	
3.	Proof of GST Registration (applicable on lead and all JV Partners, in case of exemption of any partner, the relevant exemption from relevant authority should be attached in proposal with proper justification).	
4.	Letter of Credit line of PKR 100 million from Bank for the period of one year from proposal submission date / Audited Financial Statement of Minimum Rs. 100 million budget capacity during any of the last 02 years (requirement can be filled by any of the partner individually or as a consortium)	
5.	Original affidavit (not older than one month) from lead bidder on Stamp Paper(s) of worth Rs.100 or more that each entity of the consortium is not insolvent, bankrupt and is not blacklisted or debarred by PPRA, Government, Semi-Government, Private, Autonomous body or any other international organization. Must be provided before closing time of the bid submission.	
6.	Original affidavit (not older than one month) from lead bidder on Stamp Paper(s) of worth Rs.100 or more that the Bidder is an active taxpayer and has submitted its tax return for the preceding fiscal year or provide exemption certificate. **Taxpayer list serial number (downloadable from FBR's website) is also to be mentioned.** Must be provided before closing time of the bid submission.	
7.	A formal consortium agreement not older than one month on Stamp Paper(s) of worth Rs.100 or more outlining roles, responsibilities must be submitted with the proposal.	
8.	Members of one consortium cannot be part of other consortium participating in this bidding process. Bids are to be submitted against Central Region (Punjab) on EPADS.	

9.	Bidders are required to provide list of centers along with capacity of each lab for accommodating trainees in each batch (maximum 40), the proposed centers should be located in geographical boundaries as defined in Central Region (Punjab), any non-compliance in this regard shall lead to disqualification.	
10.	Undertaking from lead bidder on letter head that all items / services will be delivered within agreed timelines after the issuance of purchase order/Contract Signing. Failing to provide items / services within agreed timelines, a penalty will be levied as mentioned in this document.	
11.	Lead partner or one of the consortium partners must have presence in the Central Region (Punjab).	
12.	**"TECHNICAL PROPOSAL – *Procurement of Services for Upskilling Training Program for the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I"*** Technical Proposal must be submitted on E-Pads (https://eprocure.gov.pk/). Bidders are to make sure that Financial Proposal is **not** part of the Technical Proposal in any form otherwise the bid will be rejected..	
	"FINANCIAL PROPOSAL - *Procurement of Services for Upskilling Training Program for the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I"* Financial Proposal must be submitted on E-Pads (https://eprocure.gov.pk/). The Financial Proposal should not be part of Technical Proposal in any form otherwise the bid will be rejected.	

Note: Bidders are required to submit *filled, signed & stamped copy of the above checklist* along with the Proposal.

5.7 Penalty

Failing to provide items / services within agreed timelines, a penalty will be levied as follows:

Deliverable	Parameter	Requirements	Penalty
Delivery of the trainings as per PO / contract	Training as per agreed course curriculum and timeframe to complete the trainings number	Agreed timeframe (in Weeks)	Delay up to 04 weeks after scheduled date @1.0% and beyond 04 weeks' penalty will be 2% of PO value. Week means full week (7 days). If delay is more than 8 weeks from the scheduled date, authority reserves right to cancel the order.

Based on justifiable reasons, the Project Steering Committee may extend the timelines of deliverables.

5.8 Technical Evaluation Criteria

During the technical evaluation no amendments in the Proposals shall be permitted. Bidders who obtain at least 70% marks in general and 100% Conformity to the Course Curriculum in technical evaluation criteria will qualify and Financial Proposals would be opened only for technically qualified Bidders.

Financial Proposals of those Bidders obtaining less than 70% marks in general and 100% in conformity to the course curriculum shall remain un-opened and will be returned to the Bidders. An evaluation committee appointed by the executing agency will evaluate Technical Proposals based on their compliance with the RFP and by applying the evaluation criteria and the point system, specified below:

Sr #	Description	Max. Score	Marks Allocation	Means of Verification
1	Firm/Bidder Profile (Registered age)– **(Form B2)**	10	01 mark per year (Max. 10 Marks)	Certificate of Incorporation / Registration documents (Lead firm's age will be considered)
2	Experience of Consortium in Conducting Similar Trainings/ Courses • (Total No. of (50-200) Trainees or Students • 30 days' duration of each) in the field of semiconductor and IC chip design. **(Form B3)**	30	• 15 marks for Training related to semiconductor and chip design: (3 Marks for each training)	• Purchase Orders / Completion certificate and/or signed contracts shall be attached as evidence • (Experience of all JV members consolidated). For Courses (Industry approved course outline is required).
			• 15 marks for Course's related to semiconductor and chip design: (3 Marks for each course (UG & PG level)	
3	Qualification and Competence of the proposed Team Members–Full Time/Part time/ **(Form B4-I & B4-II).**	20	Relevant work experience of team lead (One project (chip design project / training)) =1.0 mark) (Maximum 5 marks)	CV to be provided on Form – B4-I
			Relevant experience of the team deployed on this assignment (training on IC Chip	Team composition to be provide on Form B4-II and details to be

			Design and Verification) 3 marks for each team member (Maximum 15 marks). Following is the bifurcation of marks: a) Education and qualifications in relevant field [1 mark maximum] i. 18 years of Education (1 mark) ii. 16 years of Education (0.5 mark) b) Relevant Work Experience [1 mark maximum] i. Number of similar projects / trainings (0.2 marks for each project / training) c) Relevant Professional Certifications [1-mark maximum] i. 0.5 marks for each certification	provided on Form B4-I.
4	Training Methodology	30	The trainings methodology shall include: a. Training Delivery Structure b. Curriculum Integration c. Practical Components d. Assessment and Evaluation e. Soft Skills & Career Support f. Component wise work plan & Timelines	Detailed Write-up to be provided for each component. **(Form B-5-III)**

			(each component carries 05 marks)	
5	Financials Strength of the Bidder (requirement can be filled by any of the partner individually or as a consortium).	20	Average annual Budget of the last 2 years is more than 500 million (20 marks)	Audited Financial Statements for the last two years issued by an external auditor.
			Average annual Budget of the last 2 years is more than 300 million (10 marks)	
			Average annual Budget of the last 2 years is more than 100 million (5 marks)	
6	Transfer of Knowledge	10	Submission of training plan for PSEB's designated staff (3 marks)	Submitted Training Plan & Manuals
			Detailed Training Manuals (7 marks)	
7	Physical & ICT Infrastructure	20	a. Labs equipment relevant to the nature of training (05 Marks) b. Classroom infrastructure (05 Marks) c. EDA Tools availability (10 Marks)	Inventory List, Photographs, Licenses for EDA Tools (Form B5-I)
8	Industry engagement / support letters	10	Support Letters/MoU/Agreement signed with IC Chip Design/Verification companies working in relevant Industry of the project (02 Marks for each)	Support Letters / MOUs / Agreements
9	Inclusivity	05	• Inclusion of women, minorities, and differently-abled trainees. (2.5 marks)Participation consortium members	A supporting write-up is required to be furnished with the proposal (Form B5-II)

			from Tier-II or Tier-III cities (2.5 marks)	
10	Presentation / Demonstration of the Proposed Solution	20	Onsite presentation of proposed solutions by participating bidders / consortium	
	G. Total	**175**		

Note: Minimum **70%** will be qualifying marks of total Technical Evaluation Marks.

5.9 Final Ranking and Award Decision

After completion of both technical and financial evaluations, the proposal with the highest combined score (out of 100%) will be recommended for award, provided it meets all mandatory compliance and legal requirements.

6. Instructions for Bidders

This document contains all the information pertinent to this solicitation and governs the preparation and submission of Proposals. The technical & financial forms to be filled by Bidder for this assignment are annexed with this RFP document. Proposals must be submitted by the deadline, completed on the formats provided by the Company, with supporting documents, according to the guidelines given in the section titled Instructions & Information for Bidders. Selection of Bidders will be on Quality and Cost Based Selection methodology as provided in the Bidding Document.

Proposals must be clearly labeled to indicate the subjective RFP being addressed. The proposal must be supported by a separate Technical Proposal and a separate Financial Proposal, submitted on EPADS.. Single Firm / consortium can apply.The contracts will be awarded based on most advantageous bid..

Based on the availability of allocated funds, PSEB reserves the right to determine the number, scope, and nature of training programs to be delivered under this RFP. The selection and rollout of programs will be guided by strategic priorities, institutional readiness, and alignment with USTP objectives. PSEB may choose to implement select training tracks or modules from the proposed curriculum depending on budgetary constraints and performance evaluations. This approach ensures optimal utilization of resources while retaining flexibility to address evolving skill gaps and industry demands during project execution.

7. Bidding Document

The Bidder is expected to examine all instructions, general conditions, forms, terms and specifications contained in the RFP document and its annexures. Failure to comply with instructions will be at the Bidder's risk and may affect the evaluation of the Proposal. Proposals that do not comprehensively address the Scope of Work/ToR and other requirements may be

rejected. Inability to comply with applicable instructions, general conditions of contract, terms and specifications may lead to rejection of Proposal.

8. Preparation of Proposal

8.1. Language of the Proposal

Proposals prepared by the Bidders and all correspondence and documents relating to the Proposal exchanged between the Bidders and the Company shall be in writing and in English Language.

8.2. Proposal Currency

All prices shall be quoted in Pakistan Rupees (PKR) and all payments will be made in Pakistan Rupees (PKR.).

8.3. Period of Validity of Proposal

Proposals shall remain valid for 180 days from the last date of proposal submission as provided in the RFP document. In exceptional circumstances, the procuring agency may solicit the Bidder's consent to an extension of the period of validity without any material changes in the Bidding Document.

8.4. Supporting Documents

While preparing the Technical Proposal, the Bidder shall ensure that it provides the Company with documentary evidence. Bid evaluation committees will evaluate Proposals solely on the basis of documentary evidence submitted in accordance with evaluation criteria described in this Bidding Document.

8.5. Cost of Preparing Proposal

All costs of preparing Proposal and of negotiating with Company, including visits for discussion with Company, are the sole responsibility of the bidding consortium and not reimbursable.

8.6. Proposal Documents

The Proposal, with serial number of each page should comprise the following:

Technical Proposal
Technical Proposal must consist of the following: a) **Checklist** (Mandatory Documents required with the Proposal) b) Technical Proposal Submission – Form B1 c) Firms/Bidders Profile – Form B2 d) Relevant Experience of the Firm/Bidder – Form B3 e) Qualification, Total Experience and professional Certification/Membership – Form B4-I f) Composition of Proposed Project Management Team with Organogram – Form B4-II g) Details of Physical & ICT Infrastructure – Form B5-I h) Inclusivity – Form B5-II i) Training Methodology – Form B5-III

Technical Proposal shall detail the capability and experience of delivering the services specified in the ToR.. Team structure proposed by the Bidder for the project (including updated CVs of individuals involved in management and project implementation) in accordance with relevant *Forms.*
Financial Proposal
Financial Proposal must consist of the following: a) Financial Proposal Submission Form– Form C1 b) Summary of costs – Form C2 c) Format of Financial Bid – Form C3

8.7. Format and signing of Proposal

The Proposal shall be submitted on EPADS and should not contain interlineations, erasures, or overwriting, except, as necessary to correct errors made by the Bidder, in which case such corrections shall be initialed by Bidder's authorized person. The Proposals shall be clear and elaborate.

Note: *The Technical Proposal must not contain any pricing information whatsoever. Non-compliance will lead to rejection of the Proposal.*

8.8. Submission, Receipt, and Opening of Proposal

Technical and Financial Bids shall be in English language. Single Stage Two Envelop Bidding Procedure will be used by adopting Quality and Cost Based Selection for the subject procurement.

8.8.1. Bids should be submitted electronically ONLY through EPADS. Manual submission of bids is NOT allowed.

8.8.2. For registration and training on EAPDS or in case of any technical difficulty in using EPADS, prospective bidders may contact PPRA Team, Director MIS Room No.109, 1s' Floor, FBC building Sector G-5/2, Islamabad. Contact Number 051-111-137-237.

8.8.3. The bids, prepared in accordance with the instructions in the bidding documents along with bid security instrument (Copy) & Proof of Eligibility documents as specified in bid documents in favor of the undersigned must be submitted through EPADS by **April 22nd, 2026 at 03:00PM**. Bids will be opened on the same date at **03:30 PM**.

8.8.4. Technical bid mentioned with "Procurement of Services for Upskilling Training Program for National Semiconductor Design National Semiconductor Human Resource Development Program (NSHRDP) Phase-I Central Region (Punjab)" containing technical specifications only (without prices).

8.8.5. Financial proposal shall be mentioned with "Procurement of Services for Upskilling Training Program for National Semiconductor Design National Semiconductor Human Resource Development Program (NSHRDP) Phase-I Central Region (Punjab)containing the financial proposal.

8.8.6. The scanned copy of the earnest money of PKR 3,390,000/- in the shape of Bank Draft / Pay Order shall be in favor of "Pakistan Software Export Board" and shall be included in Technical Proposal.

Note: Original Bid Security instrument MUST BE submitted to the under signed before closing hours of the bids submission date and time otherwise the bid will be rejected.

9. Delivery Timeline

To ensure timely execution and alignment with the objectives of the National Semiconductor Human Resource Development Program (NSHRDP), the selected vendor is required to complete the entire delivery within the stipulated training program within timeline.

9.1. Training Delivery and Implementation Period

- All approved training programs, including curriculum setup, trainer mobilization, lab readiness, and provisioning of required software tools, must be started within the agreed timelines in the contract and from the date of contract award.

- Any delay beyond the stipulated timeline will result in liquidated damages or penalties as per the contract terms as mentioned under clause#5.7, unless officially extended by PSEB due to documented force majeure circumstances or approval of Project Steering Committee.

9.2. Commissioning Requirements

The commissioning process for the Upskilling Training Program shall include:

- Full implementation of the approved curriculum, including integration of industry-aligned modules.
- Verification of training facilities, labs, and software tools required for the program.
- Deployment and configuration of any required digital learning platforms and access credentials for all trainees.
- Submission of a commissioning checklist and training readiness report to PSEB.
- No batch will be commenced without the explicit approval of PSEB's designated authority.

9.3. Acceptance Testing

Final acceptance of the training program will be contingent upon:

- On-site validation of training facilities and resources by PSEB's designated representatives.
- Successful delivery of a trial training session to evaluate trainer preparedness and content quality.
- Demonstration of trainee access to all required tools, platforms, and materials.

- Formal sign-off from the NSHRDP Technical Lead and Program Coordinator confirming readiness to commence full-scale training.

10. Terms and Conditions

All bidders are required to review and comply with the following general and specific terms and conditions of the RFP. These terms shall form the basis of the contractual agreement with the selected vendor. PSEB reserves the right to accept or reject all proposals, without incurring any liability to the bidders.

11. Payment Terms

- Payments shall be released in accordance with approved milestone deliverables as given under clause# 5.2.3 and upon the final acceptance by the designated evaluation committee.

12. Force Majeure

- If either party is temporarily rendered unable, wholly or in part by Force Majeure to perform its duties or accept performance by the other party under the Contract it is agreed that on such party, giving notice with full particulars in writing of such Force Majeure to the other party within 14 (fourteen) days after the occurrence of the cause relied on, then the duties, of such party as far as they are affected by such Force Majeure shall be suspended during the continuance of any inability so caused but for no longer period and such cause shall as far as possible be removed with all reasonable speed. Neither party shall be responsible for delay caused by Force Majeure.
- The terms "Force Majeure" as used herein shall mean Acts of God, strikes, lockouts or other industrial disturbance, act of public enemy, war, blockages, insurrections, riots, epidemics (including operational disruptions due to government imposed COVID-19 restrictions), landslides, earthquakes, fires, storms, lightning, flood, washouts, government imposed restrictions due to environmental hazards, civil disturbances, explosion, Governmental Export/Import Restrictions, Government actions/restrictions due to economic and financial hardships, change of priorities and any other causes similar to the kind herein enumerated or of equivalent effect, not within the control of either party and which by the exercise of due care and diligence either party is unable to overcome.
- If a Force Majeure situation arises, the Bidder shall promptly notify PSEB in writing of such conditions and the cause thereof. Unless otherwise directed by PSEB in writing, the bidder shall continue to perform its obligations under the Contract as far as is reasonably practicable and shall seek all reasonable alternative means for performance not prevented by the Force Majeure event.

13. Submission Instructions

Bidders must submit their proposals on E-Pad in accordance with the instructions below. Failure to comply with these instructions may result in the rejection of the proposal.

14. Pre-Bid Meeting

A pre bid meeting will be held on 15th April, 2026 at 3:00 pm. Participating firms/consortiums are encouraged to join the meeting through the following zoom link.

Topic: Pre bid meeting for Ustp center region (punjab)
Time: Apr 15, 2026 03:00 PM Asia/Karachi
Join Zoom Meeting
https://zoom.us/j/93588923696?pwd=9Z9vuQm2fHX0ZvQ3a8CaFwRnsZMKuK.1

Meeting ID: 935 8892 3696
Passcode: 791265

15. Submission Address
All proposals must be uploaded on E-Pad to the following address:
https://eprocure.gov.pk/
16. Contact info for Queries
For any technical queries, following contact may please be approached:

Mr. Muhammad Ashraf,
Assist. Director, PSEB
Email: mashraf@pseb.org.pk

For general queries, please contact:

Mr. Rao Muhammad Arif Khan
Manager Procurement
Email: rarif@pseb.org.pk
Pakistan Software Export Board, 6th Floor New State Life Building, Blue area, Islamabad

PART B- TERMS OF REFERENCE

17. Terms of Reference

The Successful Bidder (Training Provider) is expected to deliver the following services:

17.1. Comprehensive Program Delivery & Support

The training provider shall ensure uninterrupted delivery of the approved Upskilling Training Program, including:

- Continuous academic and technical support for the duration of the training program.
- Access to trainers, mentors, and industry experts for participant guidance.
- Provision of up-to-date learning materials, courseware, and software access as per curriculum requirements.
- Resolution of trainee queries and training-related issues within agreed turnaround times.
- Support for final project execution, including access to relevant tools, platforms, and resources.
- Facilitation of industry-driven activities such as guest lectures, seminars, and mentorship sessions.
- Submission of periodic training progress reports and attendance records to PSEB.
- Enabling successful completion of industry-aligned projects and ensuring trainees meet competency benchmarks.
- Providing post-training support for at least 3 months, including career guidance and placement facilitation.

17.2. Maintenance of Training Infrastructure & Resources

- Ensure that all training facilities, labs, equipment, and software remain fully operational throughout the program.
- Provide immediate troubleshooting and resolution in case of equipment/software failures or content access issues.
- Maintain backups of course materials, project data, and assessments.
- Guarantee access to online learning platforms and tools without interruption.
- Clearly indicate the point(s) of presence in Pakistan for training support and coordination.

PART C – FORMS TO BE SUBMITTED WITH THE PROPOSAL

18. Technical Proposal - Standard Forms

- B1 - Technical Proposal Submission
- B2 - Firms/Bidders Profile
- B3 - Relevant Experience of the Firm/Bidder,
- B4-I - Qualification, Total Experience and professional Certification/Membership
- B4-II- Composition of Proposed Project Management Team with Organogram
- B5-I - Details of Physical & ICT Infrastructure
- B5-II – Inclusivity
- B5-III – Training Methodology

18.1. B1. Technical Proposal - Submission Form

To: Project Director
Pakistan Software Export Board
6th Floor New Statelife Building, Blue area, Islamabad
Islamabad, Pakistan
Tel: +92-51- 111 333 666
Fax: +92-51- 921-9075
Email: NSHRDP@pseb.org.pk
Islamabad, Pakistan

Sir,

We, the undersigned, offer to provide the services for execution of **"Procurement of Services for Upskilling Training Program for the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I)"** in accordance with your Request for Proposal dated **April 01st 2026**. We are hereby submitting our Proposal, which includes this Technical Proposal and Financial Proposal on E-Pads (https://eprocure.gov.pk/) (https://eprocure.gov.pk/).

Our Technical Proposal shall be binding upon us subject to the modifications resulting from Contract negotiations, up to expiration of the validity period of the Proposal, which is 180 calendar days from the last date of proposal submission..

We understand you are not bound to accept any Proposal
you receive.

Yours sincerely,

Authorized Signature:

Name and Title of Signatory:
Name of Firm: Address:

18.2. B2. Lead Firm/Bidder Profile

Sr. #	Criteria	Response
1	**Profile of the agency:** i. Registered age of Firm ii. Names of Managers/ Owners/ CEO/ Directors/ Partners	
2	i. Location of Firm office/sub office ii. Number of relevant employees including their Names & Designations, Contact Numbers & Branch contact numbers	
3	**Financial Position** i. Name of Banks ii. Certificate of Financial position iii. Copy of audited Annual Accounts (of last 2 years) iv. Tax Registration (NTN/STN/FTN)	

18.3. B3. Relevant Experience of the firm/Bidder

Experience of Consortium in Conducting Similar Trainings/ Courses (Total No. of (50-200) Trainees or Students and 30 days' duration of each) in the field of semiconductor and IC chip design. Purchase Orders / Completion certificate and/or signed contracts shall be attached as evidence (Experience of all JV members consolidated). For Courses (Industry approved course outline is required).

Sr, #	Name of the training/ Course.	Name and contact details of Focal Person of Bidder	Client Name, Organization, Focal Person Name & Phone Numbers	Training/ Course duration (Start & End Date)	Number of Trainees/ Courses	Training/ Course worth in PKR.
1						
2						
3						
4						

*Please attach relevant documents to corroborate your information.

B4-I. – Qualification, Total Experience and professional Certification/Membership Personnel Summary (Complete for each Team Member)

Name of Employee:

Position		
General Information	Name:	Date of Birth:
	Telephone:	
	Fax:	
	Years with Present Employer:	

Employment Record:

Summarize overall professional experience in reverse chronological order.

DD/MM/YY		**Company/Project/Position/Specific Tech experience**

Relevant Experience:

Summarize relevant experience in reverse chronological order. Indicate particular technical and managerial experience relevant to the project / Training:

DD/MM/YY		**Company/Project/Position/Specific Tech experience**

Education:

Highest Level of Degree	**Relevance of Degree to the Assignment**
MPhil	
Masters	
Bachelors	

Certification:

Memberships:

Certification:

I, the undersigned, certify that to the best of my knowledge and belief, these data correctly describe me, my qualifications, and my experience.

_____Date: *[Signature of staff member and authorized representative of the firm] Day/Month/Year*

Full name of staff member:

_____

Full name of authorized representative:

18.4. B4-II – Composition of Proposed Project Management Team with Organogram

Sr. #	Name/ Designation	Highest Qualification/ Education	Relevant Work Experience (Projects/Trainings Delivered)	Relevant Certifications in similar fields	Proposed Role in this Project

18.5. B5-I – Details of Physical & ICT Infrastructure

Details of Physical & ICT Infrastructure including:

Sr.#	Deliverables	Status
1.	Labs equipment relevant to the nature of training	
2.	Classroom infrastructure	
3.	EDA Tools	

18.6. B5-II – Inclusivity

Sr.#	Deliverables	Number of Participants
1.	Inclusion of women, minorities, and differently-abled trainees	
2.	Participation consortium members from Tier-II or Tier-III cities. Note: Tier 2 cities are rapidly developing, medium-sized commercial hubs (e.g., Faisalabad, Multan, Sialkot, Peshawar, Rawalpindi). Tier 3 cities are smaller, developing towns with emerging market potential (e.g., Larkana, Sheikhupura, Gwadar, Abbottabad)	

18.7. B5-III – Training Methodology

1.	Training Delivery Structure	
2.	Curriculum Integration	
3.	Practical Components	
4.	Assessment and Evaluation	
5.	Soft Skills & Career Support	
6.	Component wise work plan & Timelines	

20. Compliance Sheet **Annexure-A**

100% compliance to the specification is mandatory

Course Curriculum Outlines

Digital Design & Verification Boot Camp-Level 1 - (4 Months Duration)

Target: EE & CE graduates aiming for entry level position as frontend RTL design, ASIC backend basics, and verification engineering roles.

Important Note: The training on Soft Skills will be the mandatory part of training curriculum. The soft skill should include but not limited to:

- **Module 1.** Self-grooming, Maintaining Executive Presence, Etiquettes, Ethics – 8 hrs.
- **Module 2**. Communication, Business writing – 10 hrs.
- **Module 3.** Leadership, Team building/management, empathy – 10 hrs.

Sr.#		Course Specifications	Compliance (YES/NO)
1.	**Tools Used:**	• Simulation: • Lint & CDC: • Synthesis: • Static Timing Analysis: • Place & Route (Intro): • Debug: (Use relevant tools, to deliver the module)	
2.	**Month 1 – Foundations** Goal: Build core programming and digital design skills.	C/C++ for Hardware Engineers • Basics: syntax, control structures, pointers, arrays, strings • Data structures: linked lists, queues, stacks, hash tables • OOP concepts: inheritance, polymorphism, virtual functions, lambdas • Low-level coding: bitwise operations, memory-mapped I/O simulation • Lab: Cache simulator in C++ Digital Logic Design Fundamentals • Boolean algebra, combinational & sequential logic • Finite State Machines (Moore & Mealy) • Timing concepts: setup/hold, metastability, clock domain crossing • Basic protocols: UART, SPI, I²C • Lab: FSM-based UART controller (Use relevant tools, to deliver the module)	
3.	**Month 2 – RTL Design & Industry Protocols**	RTL Design with Verilog *(Dedicated Module)* • Modules, ports, parameters, generate blocks • Combinational logic (always @(*), blocking assignments)	

	Goal: Master synthesizable Verilog RTL coding and learn common interface protocols.	• Sequential logic (always @(posedge clk), non-blocking assignments, resets)
		• FSM design patterns, avoiding latches
		• Hierarchical design & parameterization
		• Tool Flow:
		  ○ Simulate RTL
		  ○ Lint
		  ○ Synthesize
		• Lab: ALU, FIFO, and a 2-way set associative cache controller
		Industry Protocols & Integration
		• AMBA bus standards: AXI, AHB, APB
		• Protocol design considerations
		• Simple DMA engine design
		• Lab: AXI-lite slave RTL module with APB bridge
		(Use relevant tools, to deliver the module)	

4.	**Month 3 – ASIC Flow, SystemVerilog & Verification** Goal: Transition to verification coding and understand ASIC tool flows.	ASIC Design Flow • RTL → GDSII overview • Linting & CDC analysis • Synthesis & constraints • Static Timing Analysis • Floorplanning & routing basics • Lab: Synthesize AXI-APB bridge, run STA, basic floorplan SystemVerilog for Design & Verification • Synthesizable vs non-synthesizable constructs • Interfaces, modports, virtual interfaces • OOP in SV, constrained randomization • Coverage: functional & code • Assertions (SVA) basics • Lab: Layered testbench for FIFO in SystemVerilog (Use relevant tools, to deliver the module)	
5.	**Month 4 – Verification & Final Project** Goal: Build a UVM verification environment and complete a full design + verification cycle.	UVM (Universal Verification Methodology) • Testbench architecture, agent, sequencer, driver, monitor • Factory & configuration methods • Sequence items & stimulus generation • Scoreboarding & coverage closure • Register Abstraction Layer (RAL) • Lab: UVM environment for AXI-APB bridge or FIFO Final Integrated Project *(Student Choice)* Options: • Protocol controller (AXI-Stream to FIFO) • DSP accelerator (e.g., FIR filter) • Memory controller (SRAM/DDR interface, simplified)	

		• Optional: Extend a small RISC-V core with a custom instruction
		Flow:
		• Frontend: RTL coding, linting, synthesis
		• Backend: STA, simple floorplan
		• Verification: UVM environment, functional & code coverage, assertions
		• Deliverables:
		  ○ RTL & verification code in Git repo
		  ○ Synthesis scripts & reports
		  ○ Coverage reports
		  ○ Final documentation & presentation
		(Use relevant tools, to deliver the module)	

6.	Optional Short Module – Processor Architecture *(For students interested in CPU design; 1–1.5 weeks)*	• Basic 3/5-stage pipeline • Instruction decode, execute, memory, write back • Hazards & forwarding • Integration with AMBA bus Lab: Add a simple custom instruction to a small CPU core (Use relevant tools, to deliver the module)	
	Additional Skills	• Coverage closure strategies • Writing design & verification specifications • Code review best practices	

Part-B

Financial Proposal

21. Financial Proposal - Standard Forms

C1. Financial Proposal submission form
C2. Summary of costs
C3. Format of Financial Bid

Note:- It is pertinent to mention that Financial Proposal and costing any item of this RFP shall not be the part of Technical Proposal, otherwise the bid will stand cancelled

C1- Financial Proposal Submission Form

To: Project Director
Pakistan Software Export Board
6th Floor New Statelife Building, Bluearea, Islamabad
Islamabad, Pakistan
Tel: +92-51- 111 333 666
Fax: +92-51- 921-9075
Email: NSHRDP@pseb.org.pk

Sir,

We, the undersigned, offer to provide services for execution of **"Procurement of Services for Upskilling Training Program for the Project "National Semiconductor Human Resource Development Program (NSHRDP) Phase-I) Central Region (Punjab)"** project in accordance with your Request for Proposal dated XXXX 2026 and our Proposal (Technical and Financial Proposals). Our attached Financial Proposal is for the sum of **[Amount in words and figures].** This amount is inclusive of all the local taxes, duties, fees, levies and other charges applicable on our company, our sub-contractors and collaborations under the Pakistani law.

Our Financial Proposal shall be binding upon us subject to the modifications resulting from Contract negotiations, up to expiration of the validity period of the Proposal, which is 180 calendar days from the last date of proposal submission.

We understand you are not bound to accept any Proposal you receive. We remain,

Yours sincerely,

Authorized Signature:
Name and Title of Signatory:
Name of Firm:

Address:

C2. – Summary of Costs

Particulars	Pak Rupees
Total **All applicable Taxes** **Grand Total of Financial Proposal**	

Based on the availability of allocated funds, PSEB reserves the right to determine the number, scope, and nature of training programs to be delivered under this RFP. The selection and rollout of programs will be guided by strategic priorities, institutional readiness, and alignment with USTP objectives. PSEB may choose to implement select training tracks or modules from the proposed curriculum depending on budgetary constraints and performance evaluations. This approach ensures optimal utilization of resources while retaining flexibility to address evolving skill gaps and industry demands during project execution.

22. Form C3/Annexure - B - Format of Financial Bid

Cost offered below will be considered as inclusive of all type of charges and taxes. It will also be inclusive of all type of supplies and services required as per tender documents. **The cost of training shall be quoted on per trainee basis, and must include the cost of trainers, classrooms, computer labs, venues, cost of conducting and evaluating entry tests as per following format:**

Sr. No	Name of item	No. of Trainees	Cost of Training / Trainee PKR.				Total Cost PKR.
			Duration	Cost/ Trainee	GST	Unit Cost including GST	
1.	Upskilling Training Program (Level-I) as outlined under clause# 4.5	Please refer to clause# 4.3	500 hours of training per trainee				
2.	Stationery, and course content per student		for entire length of the program				
3.	Refreshment for each student for every scheduled training session		for entire length of the program				
GRAND TOTAL							

Note:

- **Based on the availability of the funds, demand from the industry and/or availability of the trainees, PSEB reserves the right to change the number of the trainees and other listed items for any of the above listed courses and stations.**
- **It is necessary to quote against the all mentioned items in Sr. No 1-3, otherwise the bid will be considered as inclusive all mentioned items.**

Authorized Signature/Stamp **Date_____**